

REMARKS

The Applicants note that the Office Action does not acknowledge new claims 30-33 added in Amendment A mailed on February 27, 2006.

It is noted that claims 24-26 are objected to but would be allowable if rewritten in independent form. Accordingly, new claim 34 is allowable claim 24 rewritten in independent form. New dependent claims 35 and 36 depend from allowable claim 34. It is believed that all of the new claims are allowable.

Claims 16-20, 22, 23 and 27-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsue, *et al.* (U.S. Patent Number 6,483,142 - hereinafter Hsue '142). Claim 21 rejected under 35 U.S.C. 102(b) as being anticipated by Hsue, *et al.* (U.S. Patent Number 6,512,260 - hereinafter Hsue '260). In view of the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention as claimed in claims 16-33, a dual damascene interconnection structure with a metal-insulator-metal includes a via level intermetal dielectric and a trench level intermetal dielectric which are sequentially stacked on a substrate. A dual damascene interconnection is formed in the via-level intermetal dielectric and the trench-level intermetal dielectric. The dual damascene interconnection includes a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric. A metal-insulator-metal capacitor is formed between the via-level intermetal dielectric and the trench-level intermetal dielectric to include a lower electrode, a dielectric layer and an upper electrode.

Claims 16-33 are amended to clarify that the dual damascene interconnection includes a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric. It is believed that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

Hsue '142 discloses dual damascene patterns including trenches 162 and vias 160 formed in insulator 158 and insulator 138, respectively, which are used for Cu wires 148a and 148b (see Hsue '142, column 6, lines 22-25). A capacitor 132 including a conducting wire 126a, a flat insulator 128a and upper electrode 130a is formed between insulator 138 and insulator 116. The conducting wire 126a is connected with a Cu wire 104a through a plug 124a formed in a via of

insulator 116. Trenches 162 of the Cu wires 148a and 148b are formed in insulator 158, the capacitor 132 is formed in insulator 138, and the plug 124a is formed in the insulator 116.

Hsue '142 fails to teach or suggest that a dual damascene interconnection structure with a metal-insulator-metal includes a via level intermetal dielectric and a trench level intermetal dielectric which are sequentially stacked on a substrate, as claimed in claims 16-33. Instead, in Hsue '142, the insulator 138, in which the capacitor 132 is formed, is formed between the insulator 158 having the trenches 162 and the insulator 116 having the plug 124a formed in the via. Further, Hsue '142 fails to teach or suggest that a dual damascene interconnection structure with a metal-insulator-metal includes a dual damascene interconnection formed in a via-level intermetal dielectric and a trench-level intermetal dielectric that includes a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric, as claimed in claims 16-33. Instead, in Hsue '142, the trench 162 is formed to the insulator 138, rather than to the insulator 116 having the via.

Hsue '142 fails to teach or suggest these elements of the invention set forth in claims 16-33. Specifically, Hsue '142 fails to teach or suggest that a dual damascene interconnection structure with a metal-insulator-metal capacitor includes a via level intermetal dielectric and a trench level intermetal dielectric which are sequentially stacked on a substrate and a dual damascene interconnection formed in a via-level intermetal dielectric and a trench-level intermetal dielectric that includes a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric, as claimed in claims 16-33. Therefore, it is believed that the claims are allowable over the cited reference, and reconsideration of the rejections of claims 16-20, 22, 23 and 27-29 under 35 U.S.C. 102(b) as being anticipated by Hsue '142, is respectfully requested.

Hsue '260 discloses dual damascene patterns including trenches 142 formed in a top portion of insulator 138 and vias 140 formed in a bottom portion of an insulator 138, a capacitor 132 formed between insulator 138 and insulator 116, and a plug 124a formed in a via in insulator 116.

Hsue '260 fails to teach or suggest that a dual damascene interconnection structure with a metal-insulator-metal includes a dual damascene interconnection formed in a via-level intermetal

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dielectric and a trench-level intermetal dielectric includes a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric, as claimed in claims 16-33. Instead, in Hsue '260, the trench 142 is formed in the top portion of the insulator 138, and, therefore, does not extend to the through the insulator 138 to the insulator 116.

Hsue '260 fails to teach or suggest these elements of the invention set forth in claims 16-33. Specifically, Hsue '260 fails to teach or suggest that a dual damascene interconnection structure with a metal-insulator-metal includes a dual damascene interconnection formed in a via-level intermetal dielectric and a trench-level intermetal dielectric includes a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric, as claimed in claims 16-29. Therefore, it is believed that the claims are allowable over the cited reference, and reconsideration of the rejections of claim 21 under 35 U.S.C. 102(b) as being anticipated by Hsue '260, is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that, upon entry of this Amendment, all claims pending in the application will be in condition for allowance. Therefore, it is requested that this Amendment be entered and that the case be allowed and passed to issue. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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